Smart Six Channel Low-Side Switch

Features

- Short Circuit Protection up to 24 V
- Over-temperature Protection
- Over-voltage Protection
- 16 bit Serial Data Input and Diagnostic Output (2 bit/ch. acc. SPI protocol)
- Direct Parallel Control of all six Channels for PWM Applications
- General Fault Flag
- Low Quiescent Current
- Compatible with 3V Micro Controllers
- **E**lectr**o**static **D**ischarge (ESD) Protection
- Parallel Inputs High or Low Active Programmable

Product Summary

Supply voltage	V_S	4.5 – 5.5	V
Drain source clamping voltage	$V_{DS(AZ)typ.}$	53	V
On resistance	R_{ON1-4}	0.25	Ω
	$R_{ON\ 5,6}$	0.45	Ω
Output current (Channel 1-4)	$I_{D(NOM)}$	2	A
(Channel 5,6)	$I_{D(NOM)}$	1	A

P-DSO 36-12
Ordering Code:
Q67007A9397A702

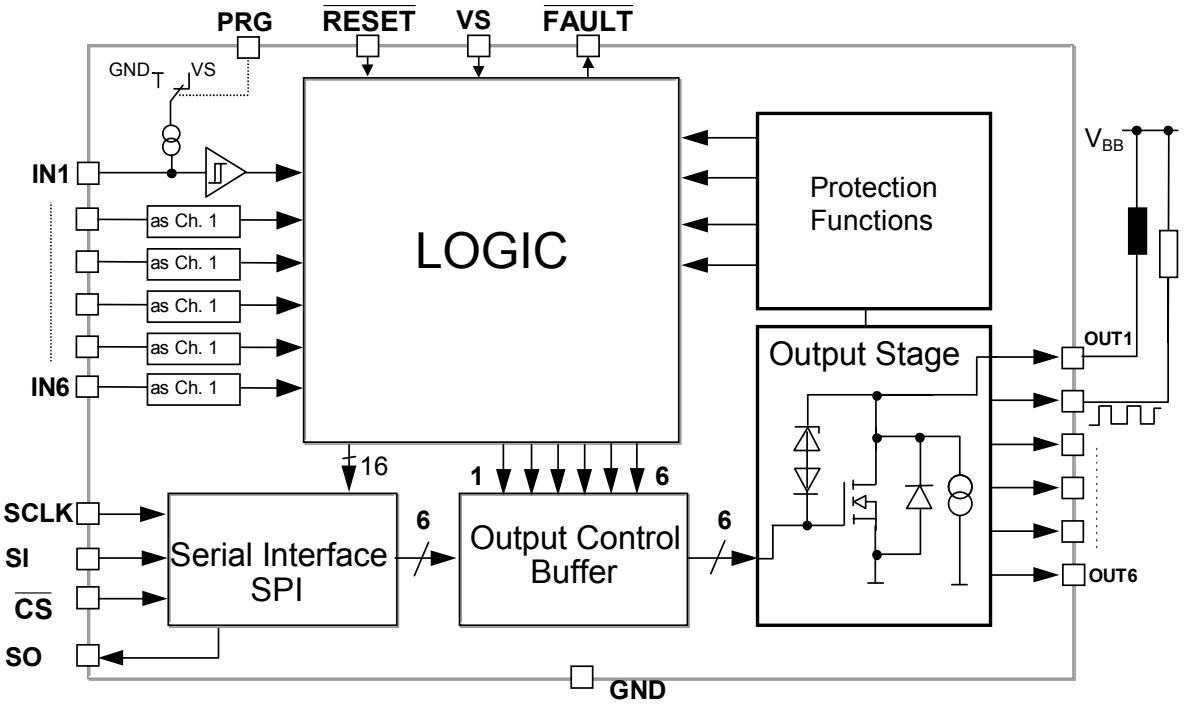
Application

- µC Compatible Power Switch for 12 V and 24V Applications
- Switch for Automotive and Industrial System
- Solenoids, Relays and Resistive Loads
- Robotic Controls

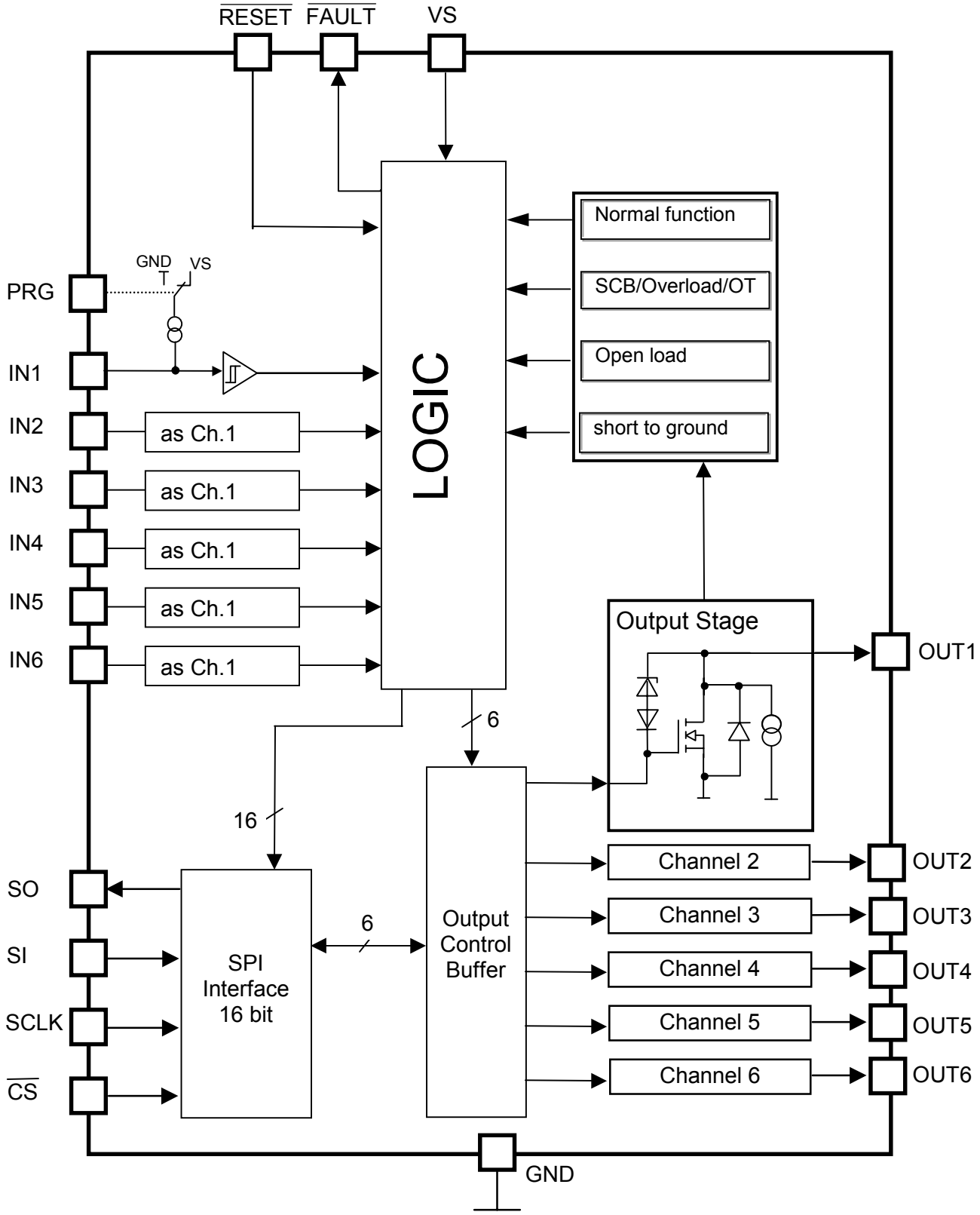
General description

Six Channel Low-Side Switch in Smart Power Technology (SPT) with a **S**erial **P**eripheral **I**nterface (SPI) and six open drain DMOS output stages. The TLE 6232 GP is protected by embedded protection functions and designed for automotive and industrial applications. The output stages are controlled via an SPI Interface. Additionally all six channels can be controlled direct in parallel for PWM applications. Therefore the TLE 6232 GP is particularly suitable for engine management and powertrain systems.

Block Diagram



Detailed Block Diagram

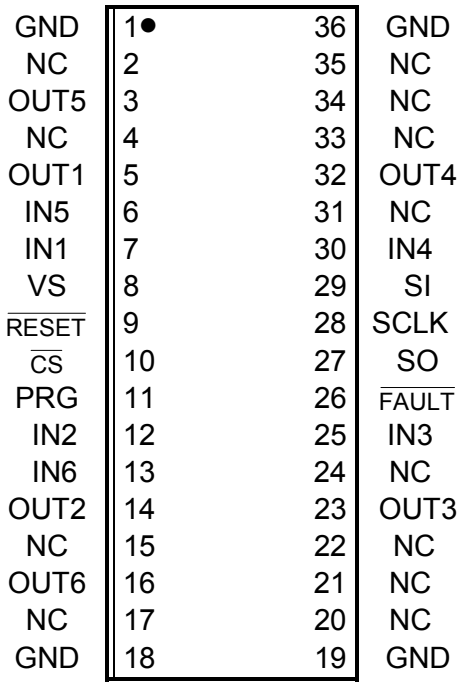


Pin Description

Pin	Symbol	Function
1	GND	Ground
2	NC	not connected
3	OUT5	Power Output Channel 5
4	NC	not connected
5	OUT1	Power Output Channel 1
6	IN5	Input Channel 5
7	IN1	Input Channel 1
8	Vs	Supply Voltage
9	$\overline{\text{RESET}}$	Reset
10	$\overline{\text{CS}}$	Slave Select
11	PRG	Program (inputs high or low-active)
12	IN2	Input Channel 2
13	IN6	Input Channel 6
14	OUT2	Power Output Channel 2
15	NC	not connected
16	OUT6	Power Output Channel 6
17	NC	not connected
18	GND	Ground
19	GND	Ground
20	NC	not connected
21	NC	not connected
22	NC	not connected
23	OUT3	Power Output Channel 3
24	NC	not connected
25	IN3	Input Channel 3
26	$\overline{\text{FAULT}}$	General Fault Flag
27	SO	Serial Data Output
28	SCLK	Serial Clock
29	SI	Serial Data Input
30	IN4	Input Channel 4
31	NC	not connected
32	OUT4	Power Output Channel 4
33	NC	not connected
34	NC	not connected
35	NC	not connected
36	GND	Ground

Heat Slug internally connected to ground pins

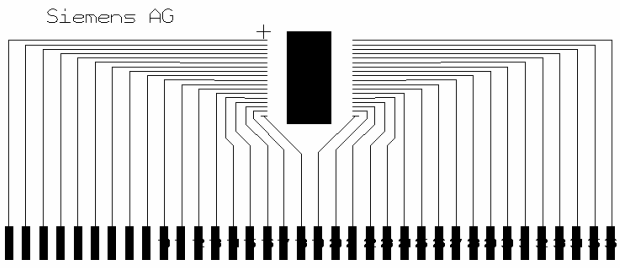
Pin Configuration (Top view)



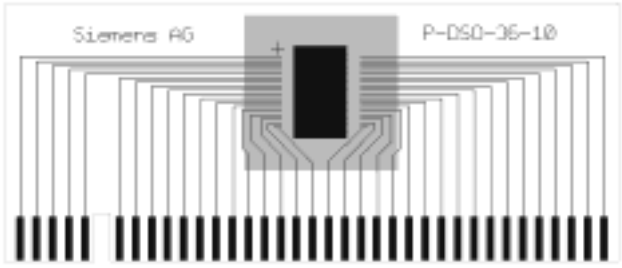
Power SO 36

Maximum Ratings for T_j = – 40°C to 150°C

Parameter	Symbol	Values	Unit
Supply Voltage	V_S	-0.3 ... +7	V
Continuous Drain Source Voltage (OUT1...OUT8)	V_{DS}	45	V
Input Voltage, All Inputs and Data Lines	V_{IN}	- 0.3 ... + 7	V
Operating Temperature Range Storage Temperature Range	T_j T_{stg}	- 40 ... + 150 - 55 ... + 150	°C
Output Current per Channel (see el. characteristics)	$I_{D(lim)}$	$I_{D(lim)\ min}$	A
Single pulse inductive Energy (internal clamping) T_j=125°C, Ch1-4: 3A linear decreasing Ch5,6: 1,5A linear decreasing	E	 40 20	mJ
Output Current per Channel @ T_A = 25°C (All 6 Channels ON; Mounted on PCB) [1)]	$I_{D\ 1\text{-}4}$ $I_{D\ 5,6}$	1.1 0.55	A
Power Dissipation (mounted on PCB) @ TA = 25°C	P_{tot}	3.3	W
Electrostatic Discharge Voltage (Human Body Model) according to MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 - 1993	V_{ESD}	2000	V
DIN Humidity Category, DIN 40 040		E	
IEC Climatic Category, DIN IEC 68-1		40/150/56	
Thermal Resistance junction – case (die soldered on the frame) junction - ambient @ min. footprint junction - ambient @ 6 cm^2 cooling area with heat pipes	 R_{thJC} R_{thJA}	 2 50 38	K/W



Minimum footprint



PCB with heat pipes,
backside 6 cm^2 cooling area

[1)] Output current rating so long as maximum junction temperature is not exceeded. At T_A = 125 °C the output current has to be calculated using R_{thJA} according mounting conditions.

Electrical Characteristics

Parameter and Conditions V_S = 4.5 to 5.5 V ; T_j = - 40 °C to + 150 °C ; Reset = H (unless otherwise specified)	Symbol	Values			Unit
		min	typ	max	
1. Power Supply, Reset					
Supply Voltage[2]	V_S	4.5	--	5.5	V
Supply Current	I_S	--	--	10	mA
Supply Current in Standby Mode (RESET = L)	$I_{S(stdy)}$	--	--	10	µA
Minimum Reset Duration	$t_{Reset,min}$	1	--	--	µs
2. Power Outputs					
ON Resistance V_S = 5 V; I_D = 1 A T_J = 25°C Channel 1-4 T_J = 150°C	$R_{DS(ON)}$	-- --	0.25 --	0.28 0.5	Ω
ON Resistance V_S = 5 V; I_D = 500 mA T_J = 25°C Channel 5,6 T_J = 150°C	$R_{DS(ON)}$	-- --	0.45 --	0.55 1	Ω
Output Clamping Voltage Output OFF	$V_{DS(AZ)}$	45	53	60	V
Current Limit Channel 1-4 Current Limit Channel 5,6	$I_{D(lim)\ 1-4}$ $I_{D(lim)\ 5,6}$	3 1.5	4 2	6 3	A
Output Leakage Current V_{Reset} = L	$I_{D(lkg)}$	--	--	10	µA
Turn-On Time Ch 1-4 I_D = 2 A, resistive load Ch 5,6 I_D = 1 A, resistive load	t_{ON}	--	5	10	µs
Turn-Off Time Ch 1-4 I_D = 2 A, resistive load Ch 5,6 I_D = 1 A, resistive load	t_{OFF}	--	5	10	µs
Switch-On Slew Rate (resistive load)	s_{on}	1	4	20	V/µs
Switch-Off Slew Rate (resistive load)	s_{on}	1	4	20	V/µs
3. Digital Inputs					
Input Low Voltage	V_{INL}	- 0.3	--	1.0	V
Input High Voltage	V_{INH}	2.0	--	--	V
Input Voltage Hysteresis	V_{INHys}	100	200	400	mV
Input Pull Down/Up Current (IN1 ... IN6)	$I_{IN(1..6)}$	10	20	50	µA
Input Pull Up Current (Reset)	$I_{IN(Res)}$	10	20	50	µA
Input Pull Down Current (PRG)	$I_{IN(PRG)}$	10	20	50	µA
Input Pull Up Current ($\overline{CS}$, SI, SCLK)	$I_{IN(SI,SCLK)}$	10	20	50	µA
4. Digital Outputs (SO, $\overline{FAULT}$)					
SO High State Output Voltage I_{SOH} = -2 mA	V_{SOH}	V_S - 1	--	--	V
SO Low State Output Voltage I_{SOL} = 2 mA	V_{SOL}	--	--	0.4	V
Output Tri-state Leakage Current $\overline{CS}$ = H, 0 ≤ V_{SO} ≤ V_S	I_{SOlkg}	-10	0	10	µA
FAULT Output Low Voltage I_{FAULT} = 2 mA	V_{FAULTL}	--	--	0.4	V

[2] For V_S < 4.5V the power stages are switched according the input signals and data bits or are definitely switched off. This under-voltage reset gets active at V_S = 3V (typ. value) and is specified by design.

Electrical Characteristics cont.

Parameter and Conditions		Symbol	Values			Unit
V_S = 4.5 to 5.5 V ; T_j = - 40 °C to + 150 °C ; Reset = H (unless otherwise specified)			min	typ	max	
5. Diagnostic Functions						
Open Load Detection Voltage		$V_{DS(OL)}$	0.52* V_s	0.6* V_s	0.68* V_s	V
Short to Ground Detection Voltage		$V_{DS(SHG)}$	0.32* V_s	0.4* V_s	0.48* V_s	V
Diagnostic Current (incl. Leakage)	$U_{OUTi,j}$ = 14V	$I_{OUTi,j}$	325	580	980	µA
	$U_{OUTi,j}$ = 0V	$-I_{OUTi,j}$	50	130	250	µA
Current Limitation; Overload Threshold Current		$I_{D(lim)\ 1\text{-}4}$	3	4	6	A
		$I_{D(lim)\ 5,6}$	1.5	2	3	A
Over-temperature Shutdown Threshold		$T_{th(sd)}$	170	--	200	°C
Hysteresis		T_{hys}	5	10	20	K
Fault Delay Time		$t_{d(fault)}$	60	120	240	µs
6. SPI-Timing						
Serial Clock Frequency (@ $C_{SO} \leq$ 50pF)		f_{SCK}	DC	--	5	MHz
Serial Clock Period (1/fclk)		$t_{p(SCK)}$	200	--	--	ns
Serial Clock High Time		t_{SCKH}	50	--	--	ns
Serial Clock Low Time		t_{SCKL}	100	--	--	ns
Enable Lead Time (falling edge of $\overline{CS}$ to rising edge of CLK)		t_{lead}	100	--	--	ns
Enable Lag Time (falling edge of CLK to rising edge of $\overline{CS}$)		t_{lag}	150	---	--	ns
Data Setup Time (required time SI to falling of CLK)		t_{SU}	20	--	--	ns
Data Hold Time (falling edge of CLK to SI)		t_H	20	--	--	ns
Disable Time		t_{DIS}	--	--	100	ns
Transfer Delay Time[3] ($\overline{CS}$ high time between two accesses)		t_{dt}	150	--	--	ns
Data Valid Time[4]	C_L = 50 pF	t_{valid}	--	--	100	ns
	C_L = 100 pF		--	--	120	ns
	C_L = 150 pF		--	--	150	ns

[3] This time is necessary between two write accesses. To get the correct diagnostic information, the transfer delay time has to be extended to the maximum fault delay time $t_{d(fault)max}$ = 200µs.
[4] This parameter will not be tested but specified by design

Description of the Power Stages

4 low side power switches for nominal currents up to 3A (power stages OUT1 to OUT4). Control is possible by input pins or via SPI. For T_J = 150°C the on-resistance of the power switches is below 500mΩ.

2 low side power switches for nominal currents up to 1.5A (power stages OUT5 and OUT6). Control is possible by input pins or via SPI. For T_J = 150°C the on-resistance of the power switches is below 1Ω.

In order to increase the switching current or to reduce the power dissipation parallel connection of power stages is possible.

Each of the 6 output stages is equipped with its own zener clamp, which limits the output voltage to a maximum of 60V. The outputs are provided with a current limitation set to a minimum of 1.5A resp. 3A. Each power stage is equipped with an own temperature sensor.

Each output is protected by embedded protection functions[5)]. In case of overload or short-circuit to U_{Batt} the current is internally limited and the corresponding bit combination is set (early warning). If this operation leads to an over-temperature condition, a second protection level (about 170°C) will change the output into a low duty cycle PWM (selective thermal shut-down with restart) to prevent critical chip temperatures.

The following faults can be detected (individually for each output):

- short to UBatt:	(SCB/overload) can be detected when switches are	On state
- short to ground:	(SCG) can be detected when switches are	Off state
- open load:	(OL) can be detected when switches are	Off state
- over-temperature:	(OT) will only be detected when switches are	On state

The fault conditions SCB, SCG and OL will not be stored until an integrated filtering time is expired (please note for PWM application). If, at one output, several errors occur in a sequence, always the last detected error will be stored (with filtering time). All fault conditions are encoded in two bits per switch and are stored in the corresponding SPI registers. Additionally there are two central diagnostic bits: one especially for over-temperature (latched result of an OR-operation out of the 6 signals of the temperature sensor) and one for fault occurrence at any output. A fault that has been detected and stored in the fault register must not be replaced by o.k.-state (11) unless it is read out by the RD_DIAG command sent by the microcontroller or an internal or external reset has been applied. I.e. the fault register will be cleared only by the RD_DIAG command.

PRG - Program pin. PRG = High (V_S): Parallel inputs Channel 1 to 6 are high active
PRG = Low (GND): Parallel inputs Channel 1 to 6 are low active.
If the parallel input pins are not connected (independent of high or low activity), channels 1 to 6 are switched OFF.
PRG pin itself is internally pulled down when it is not connected.

[5)] The integrated protection functions prevent device destruction under fault conditions and may not be used in normal operation or permanently.

The effect of the integrated under-voltage detection is similar to the effect of an external reset at pin Reset (except low current consumption):

- locks all power switches regardless of their input signals
- clears the fault registers
- resets SPI control register

Parallel Connection of Power Stages

The power stages which are connected in parallel have to be switched on and off simultaneously.

In case of overload the ground current and the power dissipation are increasing. The application has to take into account that all maximum ratings are observed (e.g. operating temperature T_J and total ground current I_{GND}, see Maximal Ratings).

The maximum current limitation value (or overload detection threshold) of the parallel connected power stages is the summation of the corresponding maximum values of the power stages ($IOUT_{(lim)x}$ + $I_{OUT(lim)y}$ + ...).

	Max. Nominal Current	Max. Clamping Energy	On Resistance
2 power stages of the same type (see note 1)	($I_{max,OUTx}$+$I_{max,OUTy}$) x 0.9	0.8 x (Ex + Ey)	$0.5xR_{ON,OUTx,y}$
3 power stages of the same type (see note 1,2)	($I_{max,OUTx}$+$I_{max,OUTy}$+ $I_{max,OUTz}$) x 0.8	0.7 x (Ex + Ey + Ez)	$0.34xR_{ON,OUTx,y,z}$
2 power stages with the same clamping voltage, but different nominal current (see note 3)	($I_{max,OUTx}$+$I_{max,OUTy}$) x 0.8	Min (Eclpx , Eclpy)	$\frac{R_{ON,OUTx}xR_{ON,OUTy}}{R_{ON,OUTx}+R_{ON,OUTy}}$

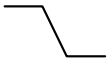
Note 1: Power stages of the same type have the same nominal current
Note 2: Only for 3A power stages
Note 3: Parallel connection of power stage type 3A/53V with type 1.5A/53V

SPI Interface

The serial SPI interface makes possible communication between TLE6232 and the microcontroller.
TLE 6232 GP always works in slave mode whereas the microcontroller provides the master function. The maximum baud rate is 5MBaud.
Applying a chip select signal at $\overline{CS}$ and setting bit 7 and bit 6 of the instruction byte to „1“ and „0“ TLE 6232 GP is selected by the SPI master. SI is the data input (Signal In), SO the data output
(Signal Out). Via SCLK (Serial Clock Input) the SPI clock is given by the master.

SPI Signal Description

$\overline{CS}$ - Chip Select. The system microcontroller selects the TLE 6232 GP by means of the $\overline{CS}$ pin. Whenever the pin is in a logic low state, data can be transferred from the µC and vice versa.



$\overline{CS}$ High to Low transition: - diagnostic status information is transferred from the power outputs into the shift register.
- serial input data can be clocked in from then on
- SO changes from high impedance state to logic high or low state corresponding to the SO bits

$\overline{CS}$ Low to High transition: - transfer of SI bits from shift register into output buffers
- reset of diagnosis register

To avoid any false clocking the serial clock input pin SCLK should be logic low state during high to low transition of $\overline{CS}$. When $\overline{CS}$ is in a logic high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

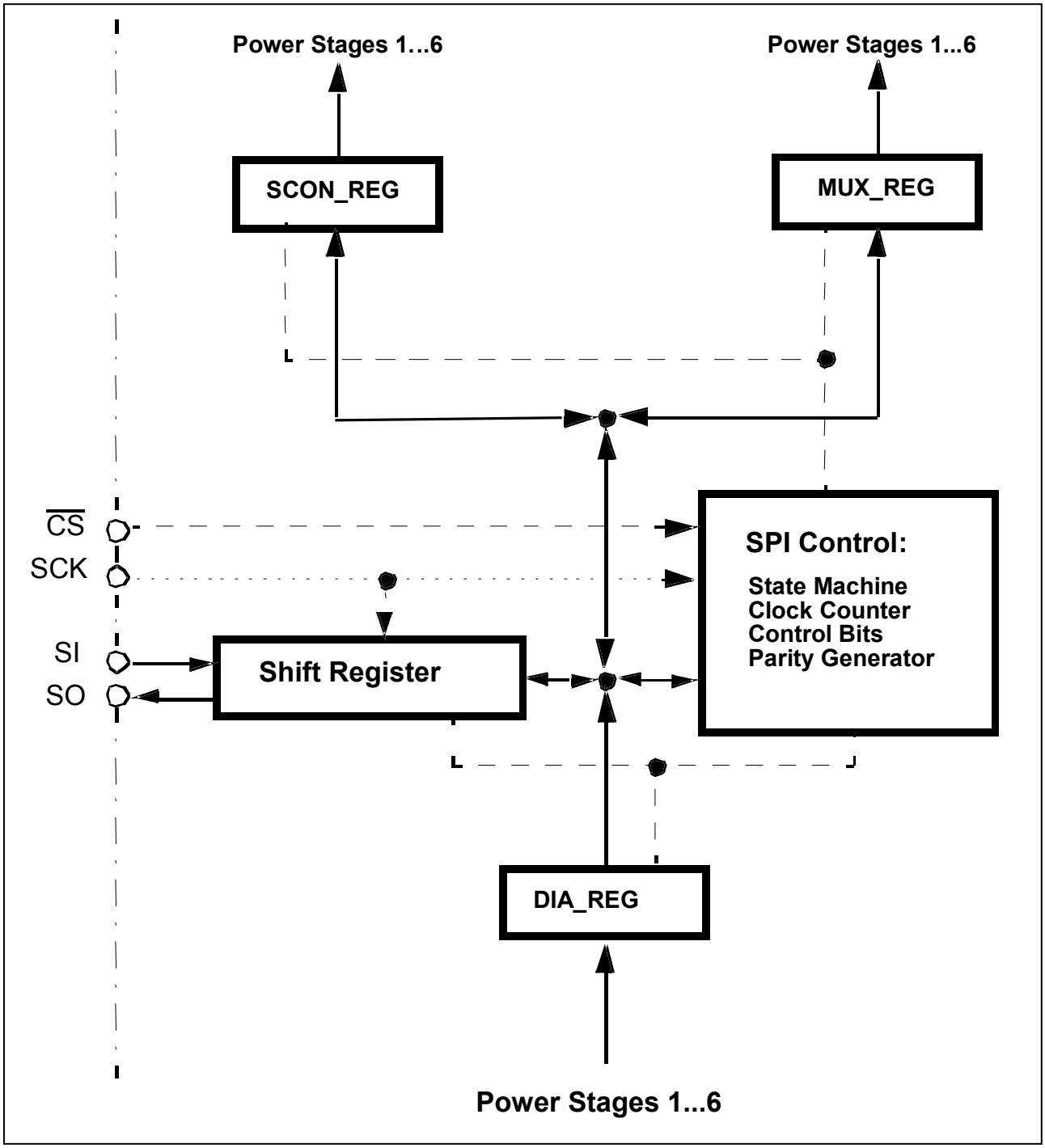
SCLK - Serial Clock. The system clock pin clocks the internal shift register of the TLE 6232 GP. The serial input (SI) accepts data into the input shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out of the shift register on the rising edge of serial clock. It is essential that the SCLK pin is in a logic low state whenever chip select $\overline{CS}$ makes any transition. The number of clock pulses will be counted during a chip select cycle. The received data will only be accepted, if exactly 16 clock pulses were counted during $\overline{CS}$ is active.

SI - Serial Input. Serial data bits are shifted in at this pin, the most significant bit first. SI information is read in on the falling edge of SCLK. Input data is latched in the shift register and then transferred to the control buffer of the output stages.
The input data consists of two bytes - a "control byte" followed by a "data byte". The control byte contains the information as to whether the data byte will be accepted or ignored (see diagnostics section). The data byte contains the input information for the six channels. A logic high level at this pin (within the data byte) will switch on the power switch, provided that the corresponding parallel input is also switched on (AND-operation for channel 1 to 6).

SO - Serial Output. Diagnostic data bits are shifted out serially at this pin, the most significant bit first. SO is in a high impedance state until the $\overline{CS}$ pin goes to a logic low state. New diagnostic data will appear at the SO pin following the rising edge of SCLK.

$\overline{RESET}$ - Reset pin. If the reset pin is in a logic low state, it clears the SPI shift register and switches all outputs OFF. An internal pull-up structure is provided on chip.
In case of inactive chip select signal (High) or bit 7 and bit 6 of the instruction byte differing from1“ and „0“ the data output SO remains into tri-state.

SPI Interface



SPI Communication

A SPI communication starts with a SPI instruction (SI control word) sent from the controller to TLE 6232 GP. Simultaneously the device sends the first SO byte back to the µC.
During a writing cycle the controller sends the data after the SPI instruction, beginning with the MSB. During a reading cycle, after having received the SPI instruction, TLE 6232 GP sends the corresponding data to the controller, also starting with the MSB.

The SPI Interface consists of three register:

- MUX_REG: 8-bit (1 byte) length for parallel operation mode (IN1 ... IN6 enabled or not)
- SCON_REG: 8-bit (1 byte) length for serial control of the outputs (serial data bits)

- DIAG_REG: 16-bit (2 byte) length. Contains the diagnostic information (2 bits per channel), a common over-temperature bit and a common fault bit.

Registers MUX_REG and SCON_REG are writeable as well as readable from the microcontroller. The DIAG_REG can only be read from the µC.

This leads to five different control bytes which are recognized by the IC. The following table shows the different modes.

		MSB LSB	MSB LSB	
WR_SCON	SI: SO:	H L L H H L X X Z Z F OT DIA6 DIA5	D6 D5 D4 D3 D2 D1 X X DIA4 DIA3 DIA2 DIA1	Write to SCON Register.
RD_SCON	SI: SO:	H L L H L H X X Z Z F OT DIA6 DIA5	X X X X X X X X SCON6 .. . SCON1 H H	Read SCON Register
WR_MUX	SI: SO:	H L H L H L X X Z Z F OT DIA6 DIA5	M6 M5 M4 M3 M2 M1 X X DIA4 DIA3 DIA2 DIA1	Write to MUX Register.
RD_MUX	SI: SO:	H L H L L H X X Z Z F OT DIA6 DIA5	X X X X X X X X MUX6 . . MUX1 H H	Read MUX Register
RD_DIAG	SI: SO	H L L L L L X X Z Z F OT DIA6 DIA5	X X X X X X X X DIA4 DIA3 DIA2 DIA1	Read DIAG Register
		SI Control Byte	**SI Data Byte**	

Note:

'X' means 'don't care', because data will be ignored
'Dx' represents the serial data bits, either being H (= OFF) or L (= ON)
'Mx' enables parallel control of channel x H (=parallel) or L (=serial)
'Z' means tri-state
'F' is the common fault flag
'OT' is the common over-temperature flag
'DIAx' is the 2 bit diagnosis information per channel

All other possible control bytes will lead to an ignorance of the data bits, but the full diagnosis information (like RD_DIAG command) is provided at the SO line. A reset of all fault registers (and OT bit) the will only be done if the RD_DIAG command was clocked in.

Characteristics of the SPI Interface

If the slave select signal at CS is High or bit 7 and bit 6 of the instruction byte differ from „1" and „0", the state machine is set on default condition, i.e. the state machine expects an instruction.

If the 5V-reset (RESET) is active, the SPI output SO is switched into tri-state.

In order to increase the possible number of SPI participants on one and the same CS signal, bits 7 and 6 of the instruction byte are fixed as shown above. While receiving the first two bits of the instruction byte the data output SO has to be in tri-state. After having received the first two bits TLE6232 has to decide if it is addressed (bit 7 = high, bit 6 = low). In this case the remaining 6 bits of the instruction byte and the data byte are accepted and the diagnostic feedback respectively the data byte content (MUX, SCON) is sent to the microcontroller. Otherwise instruction and data bits are rejected and SO remains in tri-state.
On a reading access the bit pattern of the data byte at the SPI input SI will be ignored. The first SO byte sent out simultaneously by the TLE 6232 GP always contains the common fault bit, the over-temperature bit and the diagnostic information of channels 6 and 5 (2 bits each). Depending on the SI control byte, the second SO byte contains the requested information.

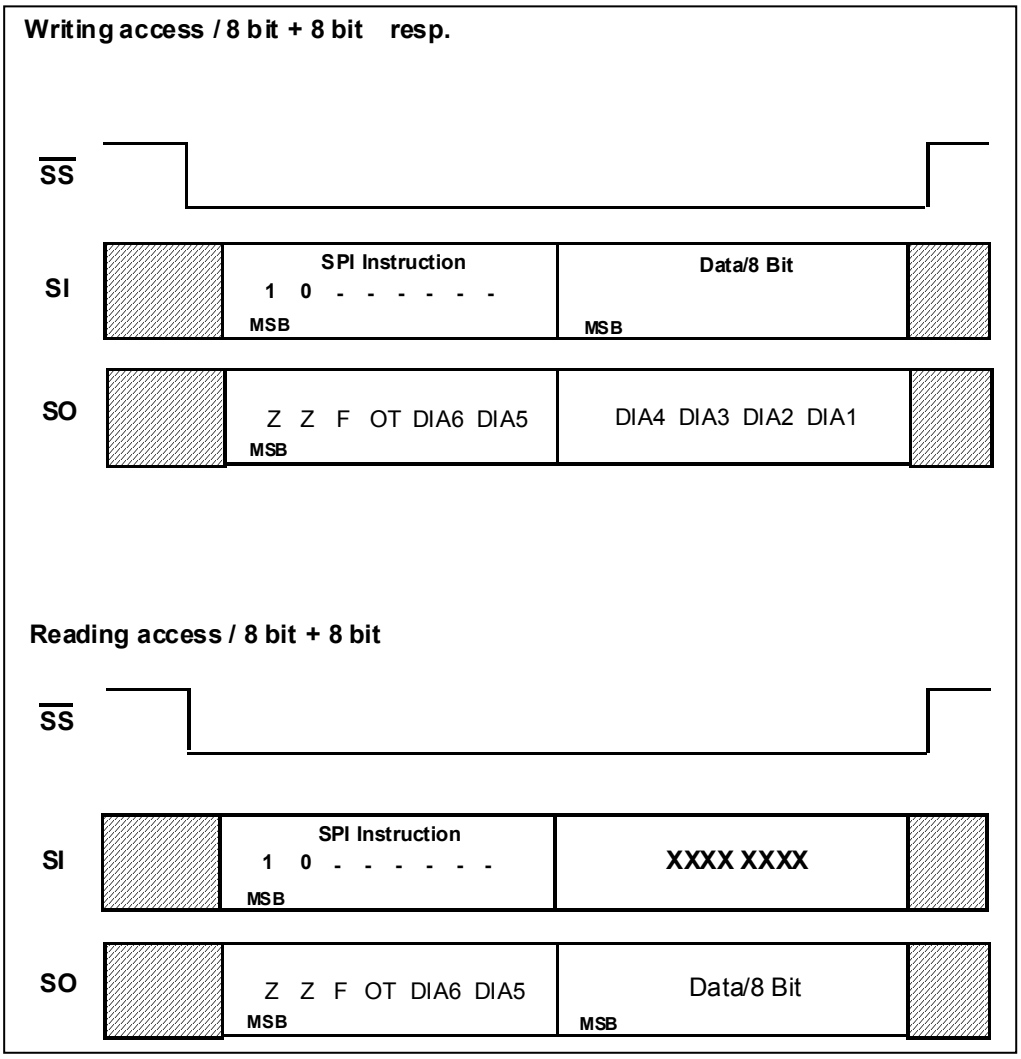
- Read back of SCON_REG (SCON bits 6 to 1 and two high bits)
- Read back of MUX_REG (MUX information for channel 6 to 1 and two high bits)
- Diagnostic information of channel 4 to 1 (2 bits per channel)

On a writing access always the full diagnostic information of the 6 channels (2 bit per channel) and the over-temperature and common fault bit is performed.

Invalid instruction/access:
An instruction is invalid, if the following condition is fulfilled:
- an unused instruction code is detected (see tables with SPI instructions).

If an invalid instruction is detected, a writing access on a register of TLE6232 GP is not allowed. In addition an access is invalid if the number of SPI clock pulses counted during active CS differs from exactly 16 clock pulses (falling edges are counted).
- On a writing access the received data is only taken over into the internal registers and
- the fault register is only cleared by the RD_DIAG command,

if exactly 16 SPI clock pulses were counted while CS active.



Serial/Parallel Control of the Power Stages 1...6

(SPI-Instructions: WR_MUX, RD_MUX, WR_SCON, RD_SCON)

The following table shows the truth table for the control of the power stages 1...6. The register MUX_REG prescribes parallel or serial control of the power stages. The register SCON_REG prescribes the state of the power stage in case of serial control.

RST	PRG	INx	MUXx	SCONx	Output OUTx of Power Stage x, x = 1..6
0	X	X	X	X	OUTx off
1	X	X	0	0	Serial Control: OUTx on
1	X	X	0	1	Serial Control: OUTx off
1	0	0	1	X	Parallel Control: OUTx on
1	0	1	1	X	Parallel Control: OUTx off
1	1	0	1	X	Parallel Control: OUTx off
1	1	1	1	X	Parallel Control: OUTx on

Note: Serial Data bits are low active. Parallel Inputs are high or low active depending on the PRG pin.

Description of the SPI Registers

Register:	**MUX_REG**						
7	6	5	4	3	2	1	0
MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	1	1
State of Reset:	FFH						
Access by Controller:	Read/Write						

Bit	Name	Description
7	MUX6	Serial or parallel control of power stage 6
6	MUX5	Serial or parallel control of power stage 5
5	MUX4	Serial or parallel control of power stage 4
4	MUX3	Serial or parallel control of power stage 3
3	MUX2	Serial or parallel control of power stage 2
2	MUX1	Serial or parallel control of power stage 1
1-0		No function: HIGH on reading

Register:	**SCON_REG**						
7	6	5	4	3	2	1	0
SCON6	SCON5	SCON4	SCON3	SCON2	SCON1	1	1
State of Reset:	FFH						
Access by Controller:	Read/Write						

Bit	Name	Description
7	SCON6	State of serial control of power stage 6
6	SCON5	State of serial control of power stage 5
5	SCON4	State of serial control of power stage 4
4	SCON3	State of serial control of power stage 3
3	SCON2	State of serial control of power stage 2
2	SCON1	State of serial control of power stage 1
1-0		No function: HIGH on reading

Diagnostics/Encoding of Failures

Description of the SPI Registers

(SPI Instructions: RD_DIAG)

Register:	**DIAG_REG1**						
7	6	5	4	3	2	1	0
ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0
State of Reset:	FFH						
Access by Controller:	Read only						

Bit	Name	Description
7-6	DIA4	Diagnostic Bits of power stage 4
5-4	DIA3	Diagnostic Bits of power stage 3
3-2	DIA2	Diagnostic Bits of power stage 2
1-0	DIA1	Diagnostic Bits of power stage 1

Note: This byte is always clocked out (second SO-byte), except the SI control words says: RD_SCON or RD_MUX. But: The content of the fault register will only be deleted if the control command 'RD_DIAG' was clocked in and 16 clock pulses were counted.

Register:	**DIA_REG2**						
7	6	5	4	3	2	1	0
Z	Z	F	OT	ST11	ST10	ST9	ST8
State of Reset:	FFH						
Access by Controller:	Read only						

Bit	Name	Description
7-6	Z	Bit 7 and 6 are always tri-state
5	F	Common error flag
4	OT	Common over-temperature flag
3-2	DIA6	Diagnostic Bits of power stage 6
1-0	DIA5	Diagnostic Bits of power stage 5

Encoding of the Diagnostic (Status) Bits of the Power Stages		
ST(2*x-1)	ST(2*x-2)	State of power stage x x = 1..6
1	1	Power stage o.k.
1	0	Overload, short circuit to battery (SCB) or over-temperature (OT)
0	1	Open load (OL)
0	0	Short circuit to ground (SCG)

Note: DIA_REG2 is always clocked out as first byte
F, OT Bit = 1: No Fault
F, OT Bit = 0: Fault, Over-temperature
The over-temperature bit is the latched result of an OR-operation out of the 6 signals of the temperature sensor)
The general fault bit shows the fault occurrence at any of the outputs.

Reset of the Diagnostic Information

The diagnostic information will only be reset after the RD_DIAG command on the rising edge of slave select or a reset signal is applied (RESET = low).

Timing Diagrams

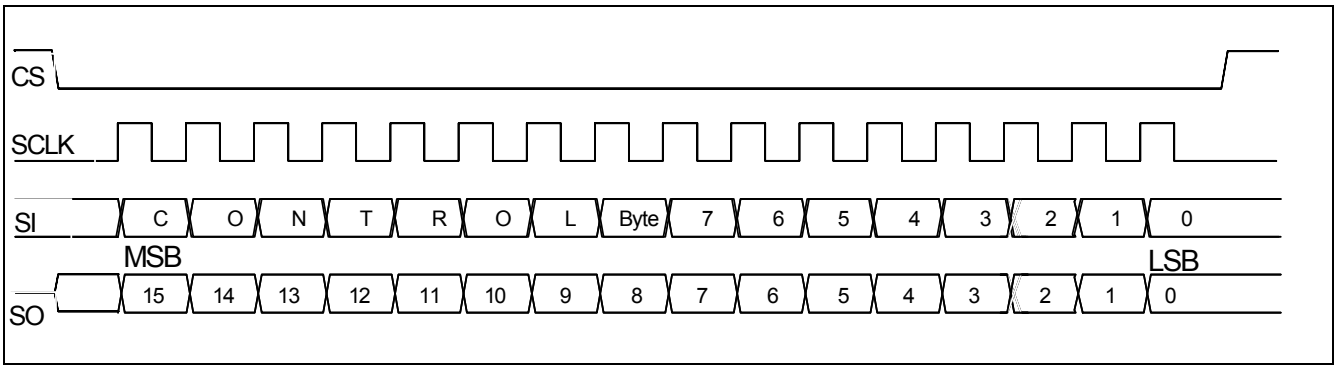


Figure 2: Serial Interface

Figure 3: Input Timing Diagram

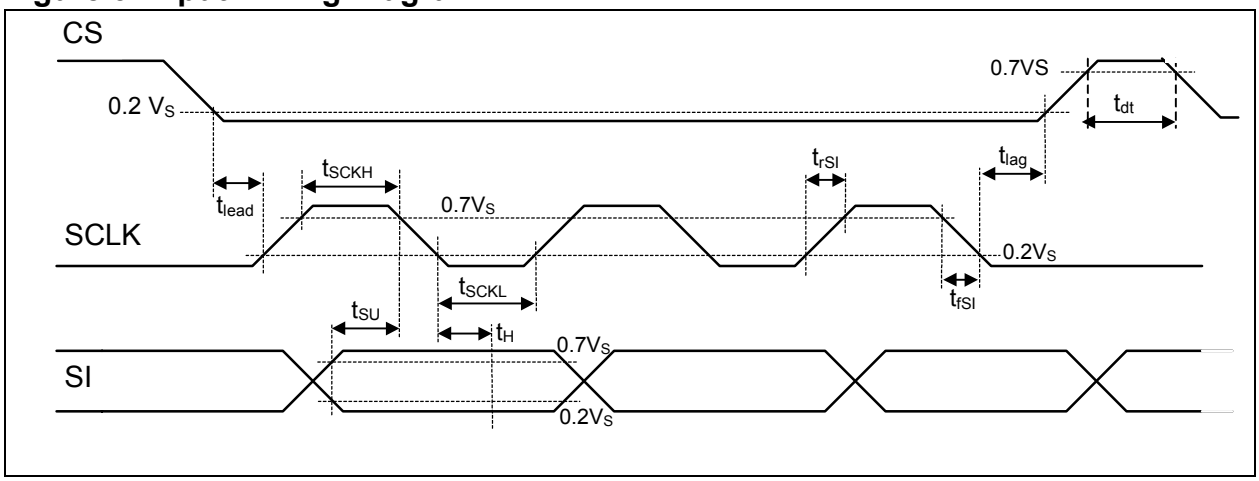
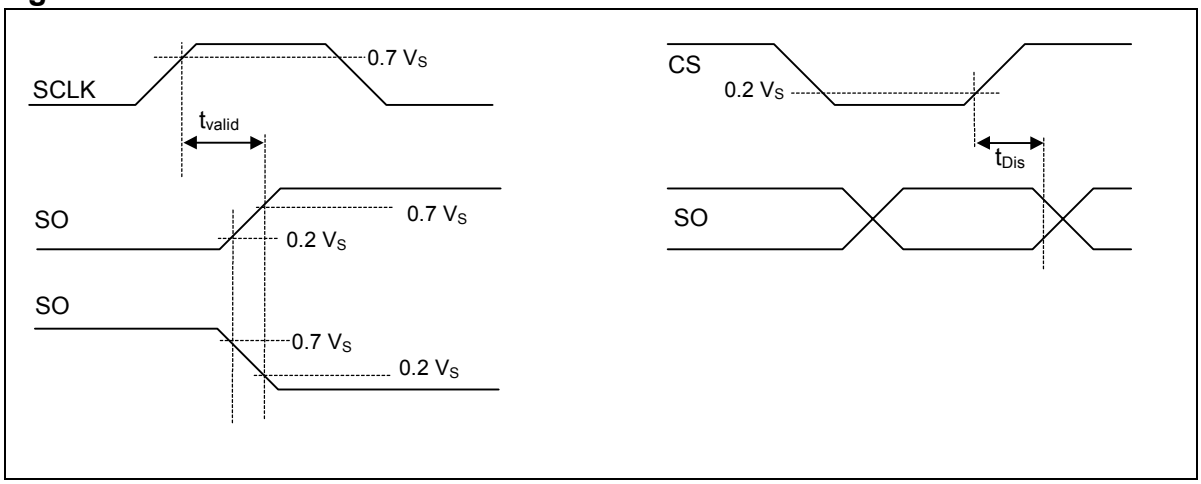


Figure 4:



SO Valid Time Waveforms **Enable and Disable Time Waveforms**

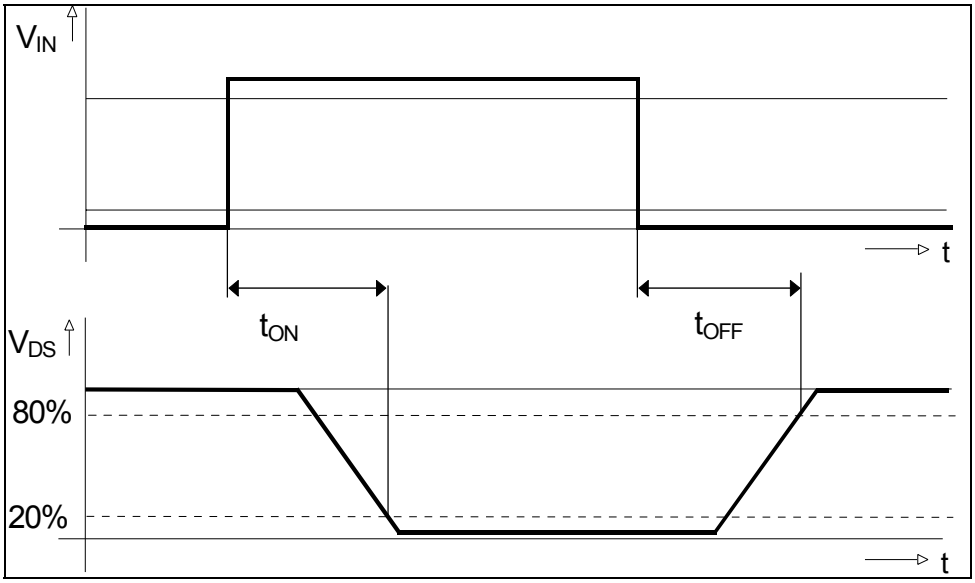
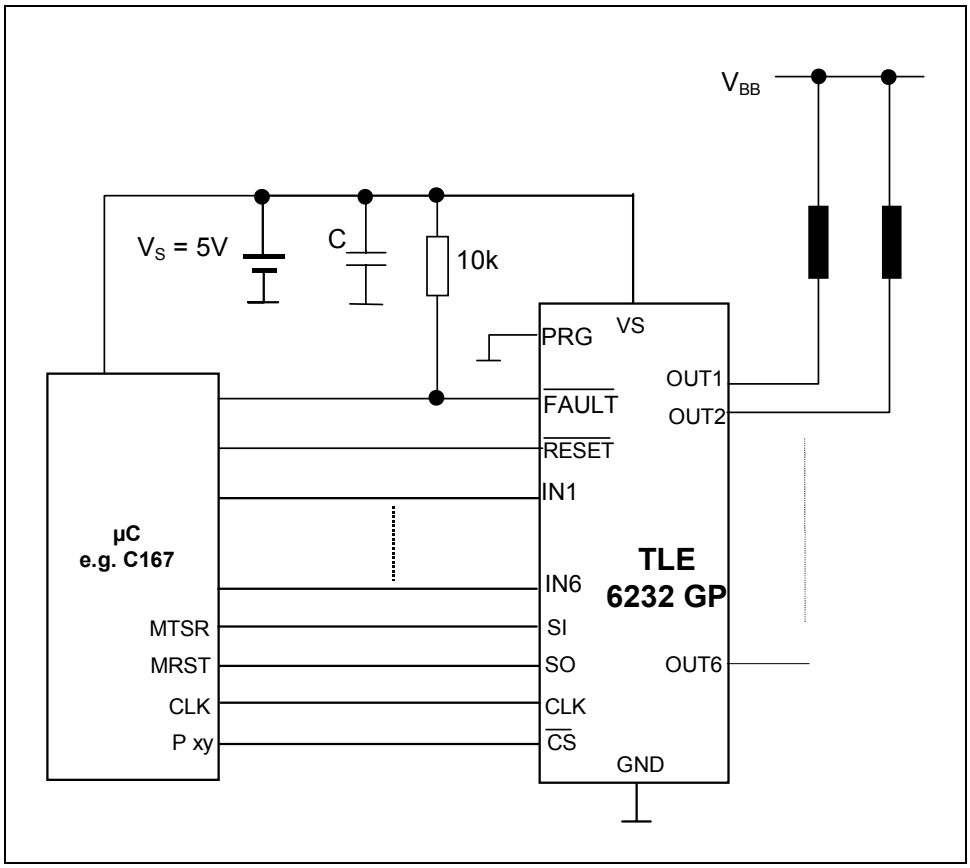


Figure 5: Power Outputs
Timing is valid for resistive load with parallel and serial control.
Rising edge of chip select initiates the switching

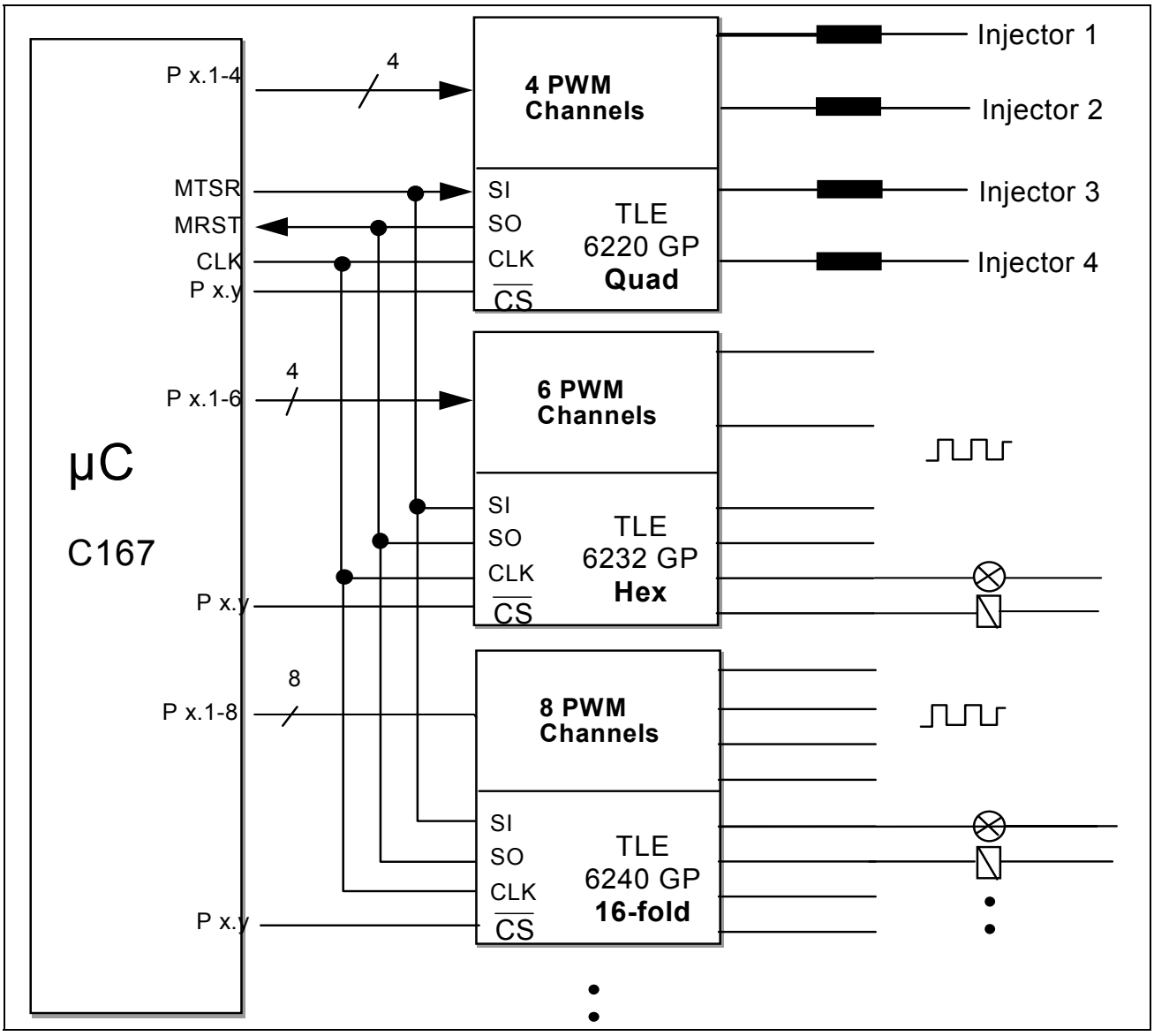
Application Circuits



Parallel SPI Configuration

Engine Management Application

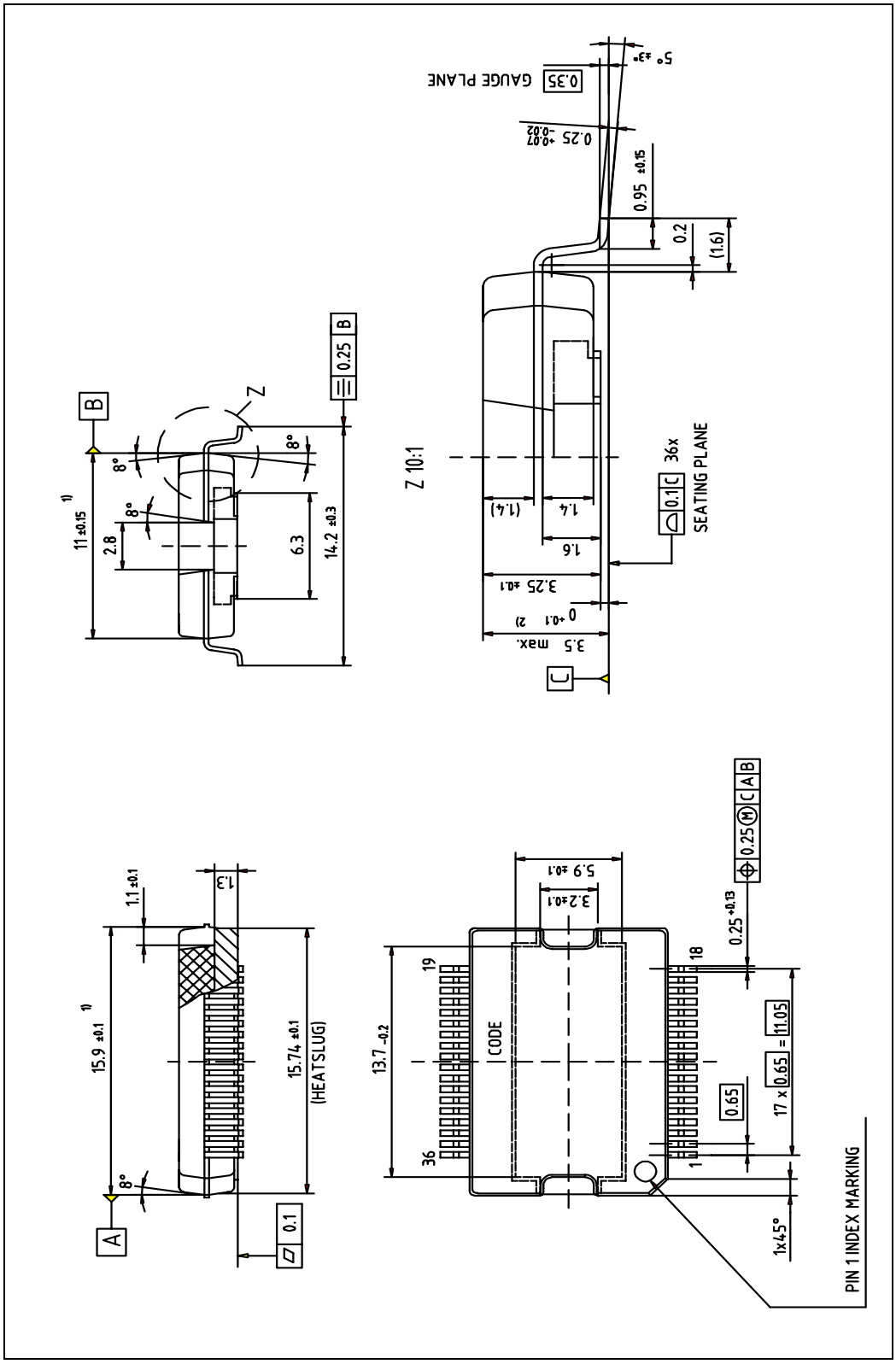
TLE 6232 GP in combination with TLE 6240 GP (16-fold switch) for relays and general purpose loads and TLE 6220 GP (quad switch) to drive the injector valves. This arrangement covers the numerous loads to be driven in a modern Engine Management/Powertrain system. From 26 channels in sum 18 can be controlled direct in parallel for PWM applications.



Package and Ordering Code

(All dimensions in mm)

P-DSO 36-12	Ordering Code
TLE 6232 GP	Q67007A9397A702



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